AMENDMENTS TO THE SPECIFICATION

Please rewrite paragraphs [0012], [0020], and [0021] of the Application as follows:

[0012] Fig. 2 shows an exemplary embodiment of a decoder driver circuit 200 of the present invention. The decoder 101 is shown as decoding a largest rectangle with an X4 designated in the upper right hand corner which symbolizes 1 of 16 memory banks. Within that rectangle is shown another rectangle with X8 also in the upper right hand corner, which designates 1 of 256 memory blocks within that memory bank. The third, smallest rectangle labeled ~~X8~~ X16 in the upper right hand corner designates 1 of 256 rows within that memory block. The decoder driver shown in Fig. 2 is used to select, by output of decoder 101, one of four memory banks, denoted by the selection rectangle X4 (201), one of two hundred and fifty-six memory blocks within a selected bank, denoted by selection rectangle X8 (203), and one of two hundred and fifty-six rows within a selected memory block denoted by ~~X8~~ X16 (205). The decoder 101 includes N-channel pass transistors N4, N5, and N6 which decode the information arriving on address lines XEN<3:0>, XB<3:0>, XA<7:0>, and XROW<7:0>. A specific wordline 228 is then selected using that address information. It should be noted that the present invention is not limited to this specific memory architecture, which is shown for illustrative purposes only.

[0020] The primary bus bridge 303 is coupled to at least one peripheral bus 310. Various devices, such as peripherals or additional bus bridges may be coupled to the peripheral bus 310. These devices may include a storage controller 311, ~~an~~ a miscellaneous I/O device 314, a secondary bus bridge 315, a multimedia processor 318, and ~~an~~ a legacy device interface 320. The primary bus bridge 303 may also be coupled to one or more special purpose high speed ports 322. In a personal computer, for example, the special purpose port might be the Accelerated Graphics Port (AGP), used

to couple a high performance video card to the processing system 300. In addition to memory device 331 which may contain a buffer device of the present invention, any other data input device of Fig. 3 may also utilize a buffer device of the present invention including the CPU 301.

[0021] The storage controller 311 couples one or more storage devices 313, via a storage bus 312, to the peripheral bus 310. For example, the storage controller 311 may be a SCSI controller and storage devices 313 may be SCSI discs. The I/O device 314 may be any sort of peripheral. For example, the I/O device 314 may be ~~an~~ a local area network interface, such as an Ethernet card. The secondary bus bridge may be used to interface additional devices via another bus to the processing system. For example, the secondary bus bridge may be an universal serial port (USB) controller used to couple USB devices 317 via to the processing system 300. The multimedia processor 318 may be a sound card, a video capture card, or any other type of media interface, which may also be coupled to one additional ~~devices~~ device, such as speakers 319. The legacy device interface 320 is used to couple legacy devices, for example, older styled keyboards and mice, to the processing system 300. In addition to memory device 331 which may contain a buffer device of the invention, any other data input device of Fig. 3 may also utilize a buffer device of the invention, including a CPU 301.

AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A decoder for driving a wordline, comprising:

a latch set to a particular state when said wordline is to be driven;

a decoding circuit for receiving and decoding the address of said wordline and setting said latch to said particular state; ~~and,~~

a first output inverter, comprising a pair of serially connected complementary CMOS transistors for providing a signal in response to the state of said latch being set to said particular state ~~driving said wordline in response to said latch being sent to said particular state~~; and

a second output inverter, connected to the output of said first output inverter, and comprising a pair of serially connected complementary CMOS transistors for driving said wordline in response to said latch being set to said particular state.

2-16. (Cancelled)

17. (New) The decoder of claim 1, further comprising:

a voltage pump for supplying a voltage to said first output inverter.

18. (New) The decoder of claim 17, further comprising:

a voltage sink, connected to said second output inverter, said voltage sink being at a potential lower than ground.

19. (New) An method of operating a wordline decoder, comprising:

decoding wordline address information and setting a latch associated with a wordline to a predetermined state when an address of said wordline is decoded;

driving signal line with an first output inverter having an input connected to an output of said latch; and

driving said selected wordline with a second output inverter having an input connected to an output of said first output inverter.

20. (New) The method of claim 19, further comprising:

supplying a voltage from a voltage pump to said first inverter for turn on said wordline.

21. (New) The method of claim 19, further comprising:

supplying a voltage sink to said second inverter for turning off said wordline.

22. (New) The method of claim 19, further comprising:

driving said selected wordline with said second output inverter to a voltage below ground when turning off said wordline.

23. (New) The method of fabricating a decoder, comprising:

fabricating a latch configured to be set to a particular state when said wordline is to be driven;

fabricating a decoding circuit for receiving and decoding the address of said wordline and setting said latch to said particular state; ~~and,~~

fabricating a first output inverter, comprising a pair of serially connected complementary CMOS transistors for providing a signal in response to the state of said latch being set to said particular state ~~driving said wordline in response to said latch being sent to said particular state;~~ and

fabricating a second output inverter, connected to the output of said first output inverter, and comprising a pair of serially connected complementary CMOS transistors for driving said wordline in response to said latch being set to said particular state.

24. (New) The method according to claim 23, further comprising fabricating a voltage pump for supplying a voltage to said first output inverter.

25. (New) The method according to claim 23, further comprising fabricating a voltage sink connected to said second output inverter.